PNET.009D

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

Tsukasa Yajima

Attn: Applications Branch

Divisional to Serial No. 09/038,749

Attorney Docket No. PNET.009D

Filed: January 25, 2001

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE (To be Amended)

PRELIMINARY AMENDMENT

Honorable Assistant Commissioner
of Patents and Trademarks,
Washington, D.C. 20231

Date: January 25, 2001

Sir:

Preliminary to the examination of the above-identified application, please enter the following amendments and remarks.

In the Abstract:

Please cancel the Abstract and replace with the Abstract attached herewith.

In the Title:

Please amend the title to read --SEMICONDUCTOR DEVICE HAVING PROTECTIVE LAYER ON FIELD OXIDE--.

In the Specification:

Page 1

Between lines 3 and 4, insert

--CROSS REFERENCE TO RELATED APPLICATIONS

This is a divisional application of application Serial No. 09/038,749, filed March 12, 1998, which is hereby incorporated by reference in its entirety for all purposes.--

Line 7, delete "a" (first occurrence).

Page 2

Line 5, after "etching" insert --of--.

Line 12, change "for" to --to--.

Page 3

Line 18, before "etched" insert --is--.

Line 20, change "scatters" to --non-uniformities--.

Page 6

Line 14, change "votage" to --voltage--.

Page 7

Line 16, after "the" insert --oxidation proof layer is exposed by removing a portion of the protective layer, so that the--.

Line 17, change "is formed" to --remains--; after "oxide" insert --.--; and delete "by".

Delete line 18.

Line 19, delete "with a removal of a part of the protective layer.".

Line 23, delete "a".

Page 11

Line 9, delete ")" (second occurrence).

Line 16, change "CPM" to --CMP--.

Page 13

Line 3, after "34" insert --(FIG. 1(f))--.

Line 18, delete "the".

Line 19, change "scatters" to --non-uniformities--.

Page 15

Line 18, change "medications" to --modifications--.

In the Claims:

Please cancel claims 1-3 without prejudice or disclaimer of the subject matter contained therein.

Please add claims 6-10 as follows:

--6. A semiconductor device comprising:

a gate formed on an active region of a substrate;

a field oxide formed on the substrate adjacent the active region;

a protective layer formed on a said field oxide, said protective layer being a material different than said field oxide;

an insulating layer formed on the substrate including said gate, said field oxide and said protective layer;

a contact hole formed through said insulating layer; and

a connecting wire coupled to said gate through said contact hole.

7. The semiconductor device of clam 6, wherein said protective layer is a polysilicon layer.

8. The semiconductor device of claim 6, wherein said protective layer is formed on said field oxide only.

9. The semiconductor device of claim 6, wherein said gate is a MOSFET gate.

10. The semiconductor device of claim 6, further comprising side walls formed on said gate, said side walls being covered by said insulating layer.--

REMARKS

Claims 4-10 are pending in the present application. Claims 1-3 have been canceled as being directed to a non-elected invention. Claims 6-10 have been presented herewith.

Favorable consideration and early allowance of the present divisional application are earnestly solicited.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

JONES VOLENTINE, L.L.C.

Andrew J. Telesz, Jr.
Reg. No. 33,581

12200 Sunrise Valley Drive, Suite 150
Reston, VA 20191
Tel. No. (703) 715-0870
Fax No. (703) 715-0877

Abstract of the Disclosure

A semiconductor device is provided with a gate formed on an active region of a substrate, with a field oxide formed on the substrate adjacent to the gate. Side walls are formed on the gate. A protective layer such as polysilicon is formed on the field oxide. Also, an insulating layer is formed on the substrate including the gate and side walls, the field oxide and the protective layer. The protective layer prevents overetching of the field oxide.